IN THE CLAIMS

1. (Previously Presented) A method for multithread processing of messages using an integrated circuit, comprising:

configuring configurable logic of said integrated circuit to have a plurality of thread circuits and an interconnection topology amongst said plurality of thread circuits, each of said plurality of thread circuits providing a control signal to each other of said plurality of thread circuits through said interconnection topology;

concurrently processing messages using said plurality of thread circuits; and

controlling operation of at least one thread circuit of said plurality of thread circuits in accordance with control data of a respective control signal from at least one other thread circuit of said plurality of thread circuits over said interconnection topology.

2. (Original) The method of claim 1, wherein each of said plurality of thread circuits comprises a state machine.

3. (Currently Amended) The method of claim 2, wherein said integrated circuit is a programmable ~~logic~~ device, and wherein said state machine of each of said plurality of thread circuits is implemented using programmable ~~logic~~ blocks of said integrated circuit.

4. (Original) The method of claim 1, wherein said controlling step comprises:

activating said at least one thread in response to said control data comprising a start command;

deactivating said at least one thread in response to said control data comprising a stop command; and

suspending said at least one thread in response to said control data comprising a suspend command.

5. (Original) The method of claim 1, wherein said control data comprises status data associated with said at least one other thread circuit of said plurality of thread circuits.

6. (Original) The method of claim 1, further comprising:

communicating data from a first thread circuit of said plurality of thread circuits to a second thread circuit of said plurality of thread circuits through said interconnection topology.

7. (Previously Presented) A method of implementing multithread processing of messages using an integrated circuit, comprising:

specifying a plurality of threads for concurrently processing messages, at least one thread of said plurality of threads including control logic for controlling operation of at least one other thread of said plurality of threads;

specifying an interconnection topology amongst said plurality of threads, at least a portion of said interconnection topology including a connection between said at least one thread and said at least one other thread, said connection including at least one control signal provided by said control logic; and

generating a physical description of a multithreading system in response to said plurality of threads and said interconnection topology, said physical description being defined in terms of components of said integrated circuit.

8. (Original) The method of claim 7, further comprising:

processing said physical description to generate data for configuring said integrated circuit with said multithreading system.

9. (Original) The method of claim 8, wherein said physical description comprises a hardware description language description.

10. (Original) The method of claim 7, wherein said control logic of said at least one thread is configured to control at least one of starting, stopping, and suspending of said at least one other thread.

11. (Original) The method of claim 7, wherein said interconnection topology further comprises a second connection for communicating data from a first thread of said plurality of threads to a second thread of said plurality of threads.

12. (Original) The method of claim 11, wherein said data is communicated in accordance with a data validity flag.

13. (Original) The method of claim 11, wherein said data is communicated in accordance with a request generated by said second thread.

14. (Previously Presented) A design tool for implementing a multithread message processing system using an integrated circuit, comprising:

means for specifying attributes of said multithread message processing system;

a first database for storing a multithread model having a thread model and an interconnection model;

a second database for storing an architecture of said integrated circuit; and

a multithread model section, comprising:

means for generating a plurality of instances of said thread model and an instance of said interconnection model in response to said specified attributes; and

means for implementing said plurality of thread model instances and said interconnection model instance in terms of said integrated circuit architecture.

15. (Previously Presented) The design tool of claim 14, further comprising:

a third database for storing a set of primitives;

wherein said specified attributes are defined in accordance with said primitives.

16. (Previously Presented) The design tool of claim 14, wherein each of said plurality of thread model instances comprises a state machine.

17. (Currently Amended) The design tool of claim 16, wherein said integrated circuit is a programmable ~~logic~~ device, and where said state machine associated with each of said plurality of thread model instances is implemented using programmable blocks ~~logic~~ of said programmable ~~logic~~ device.

18. (Previously Presented) An apparatus for multithread processing of messages using an integrated circuit, comprising:

a first configured portion within said integrated circuit for concurrently processing messages using a plurality of thread circuits, at least one of said plurality of thread circuits having control logic for controlling operation of at least one other thread circuit of said plurality of thread circuits; and

a second configured portion within said integrated circuit for providing a connection between said at least one thread and said at least one other thread, said connection including at least one control signal provided by said control logic.

19. (Currently Amended) The apparatus of claim 18, wherein said integrated circuit is a programmable ~~logic~~ device.

20. (Currently Amended) The apparatus of claim [[29]] 19, wherein each of said plurality of threads comprises a state machine implemented using programmable ~~logic~~ blocks within said programmable ~~logic~~ device.